M.2 2280 PCIe SSD 920F Datasheet

(SQF-2040-XXXECM)

CONTENTS

Revision History

Rev.	Date	History
1.0	2024/3/21	1. Preliminary release
1.1	2024/6/24	1. Added PN

1. Overview

Advantech SQFlash 920F series M.2 2280 PCIe SSD (Solid State Drive) delivers all the advantages of flash disk technology with PCIe Gen3 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. SQF 920F M.2 2280 offers a wide range capacity up to 2048GB and its performance can reach up to 3400 MB/s (for read) and 3100 MB/s (for write) based on 32CE NAND flash with 512MB/1GB/2GB DDR4. Moreover, the power consumption of SQF 920F M.2 2280 is much lower than traditional hard drives, making it the best embedded solution for new platforms.

2. Features

- **PCIe Interface**
  - Compliant with NVMe1.3
  - Compatible with PCIe I/II/III x4 interface
  - Support up to queue depth 64K
  - Support power management
- **Operating Voltage：3.3V**
- **Support LDPC with RAID ECC**
- **AES256、TCG-OPAL、TRIM、AHCI supported**
- **Temperature Ranges[1]**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -40℃ to 85℃ for storage

  *Note : 1. Based on SMART Attribute (Byte index [2 :1] of PCIe-SIG standard, which measured by thermal sensor
- **Mechanical Specification**
  - Shock：1,500G / 0.5ms
  - Vibration：20G / 80~2,000Hz
- **Humidty**
  - Humidity：Up to 95% under 55℃
- **Physical Anti temper**
  - Coating on PCBA
- **Acquired RoHS、WHQL、CE、FCC Certificate**
- **Acoustic：0 dB**
- **Dimension：80.0 mm x 22.0 mm x 3.8 mm**

3. Specification Table

■ Performance

		Sequential (MB/sec)		Random (IOPS @4K)	
		Read	**Write**	**Read**	**Write**
3D TLC	256 GB	3,200	1,300	215K	320K
	512 GB	3,400	2,400	420K	635K
	1 TB	3,400	3,100	700K	690K

* Performance measured by IOMeter with QD32, 8GB data pattern, SLC pool enable & adjustable by request.

Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (SSD Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - 3D TLC (BiCS4): 3,000 cycles
- **SSD Capacity**: SSD physical capacity in total of a SSD.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

- **Endurance measurement is based on New JEDEC 219 Client Workload and verified with following workload conditions,**
  - PreCond%full = 100%
  - Trim commands enabled
  - Random data pattern.

3D TLC	TBW	DWPD*
256 GB	320	1.14
512 GB	720	1.28
1 TB	1620	1.44

* Endurance of 1 drive writes per day (DWPD) for 3 years

4. General Description

■ Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQFlash 920F series PCIe SSD applies the LDPC with RAID ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

■ Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

SQFlash provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

■ Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. SQFlash implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

■ Power Loss Protection

– Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

■ TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

■ SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

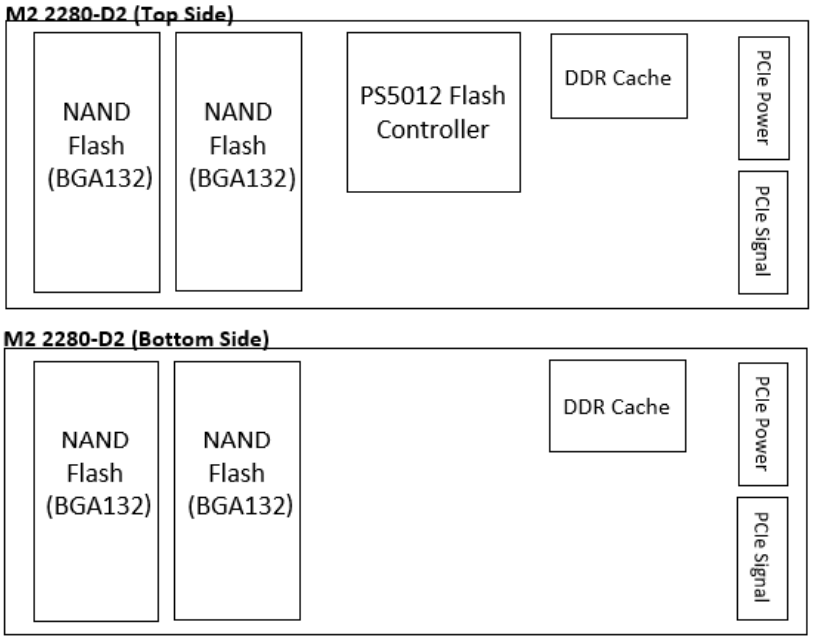
Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

Thermal Throttling

Thermal Throttling function is for protecting the drive and reducing the possibility of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to threshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below threshold temperature, the drive can resume to normal operation.

■ Block Diagram



■ LBA value

Density	LBA
256 GB	500,118,192
512 GB	1,000,215,216
1 TB	2,000,409,264

5. Security Features

Advanced Encryption Standard (AES)

An AES 256-bit encryption key is generated in the drive's security controller before the data got stored on the NAND flash. When the controller or firmware fails, the data that is securely stored in the encryption key becomes inaccessible through the NAND flash.

TCG-OPAL 2.0 Compliance

Crypto Erase is a feature that erases all data of an OPAL-activated SSD drive by resetting the cryptographic key of the disk. Since the key is modified, the previously encrypted data will become useless, achieving the purpose of data security.

Physical Presence SID (PSID) is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

6. Pin Assignment and Description

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec

50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No connect
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	N/C	PEDET (NC-PCIe)
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

7. Identify Devic Command

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 7-1 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	TBD
63:24	M	Model Number (MN)	TBD
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	TBD*
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010300
87:84	M	RTD3 Resume Latency (RTD3R)	0x001E8480 (2 Sec)
91:88	M	RTD3 Entry Latency (RTD3E)	0x00989680 (10 Sec)
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000300
99:96	M	Controller Attributes (CTRATT)	0x0002
239:100	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00
257:256	M	Optional Admin Command Support (OACS)	0x0017
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x1F
261	M	Log Page Attributes (LPA)	0x0C
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	4
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x0157 (70C)
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0161 (80C)
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0000 (No report)
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	**
311:296	O	Unallocated NVM Capacity (UNVMCAP)	**
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000
511:316	-	Reserved	non-zero
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	-	Reserved	0x0000
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x001F
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	TBD

529:528	M	Atomic Write Unit Power Fail (AWUPF)	TBD
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
703:540	M	Reserved	0x00
IO Command Set Attributes			
2047:704	M	Reserved	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	TBD
2111:2080	O	Power State 1 Descriptor (PSD1)	0x00
2143:2112	O	Power State 2 Descriptor (PSD2)	0x00
2175:2144	O	Power State 3 Descriptor (PSD3)	0x00
2207:2176	O	Power State 4 Descriptor (PSD4)	0x00
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Reserved

* The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.

** depends on the using of capacity

Table 7-2 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	TBD*
15:8	M	Namespace Capacity (NCAP)	TBD*
23:16	M	Namespace Utilization (NUSE)	TBD*
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33		Reserved	0x09
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46		Reserved	0x0000
64:48	O	NVM Capacity (NVMCAP)	0x00
103:64		Reserved	0x00
119:104	O	Namespace Globally Unique Identifier (NGUID)	TBD**
127:120	O	IEEE Extended Unique Identifier (EUI64)	TBD**
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x00000000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192		Reserved	0x00
4095:384	O	Vendor Specific (VS)	0x00

*See IDEMA SPEC

** See IEEE EUI-64 SPEC

Table 7-3 List of Identify Namespace Data Structure for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)	Byte[7:0]: Namespace Size (NSZE) (Dec)
256 GB	1DCF32B0h	500,118,192
512 GB	3B9E12B0h	1,000,215,216
1 TB	773BD2B0h	2,000,409,264

8. SMART Atrributes

■ SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

9. System Power Consumption

■ Supply Voltage

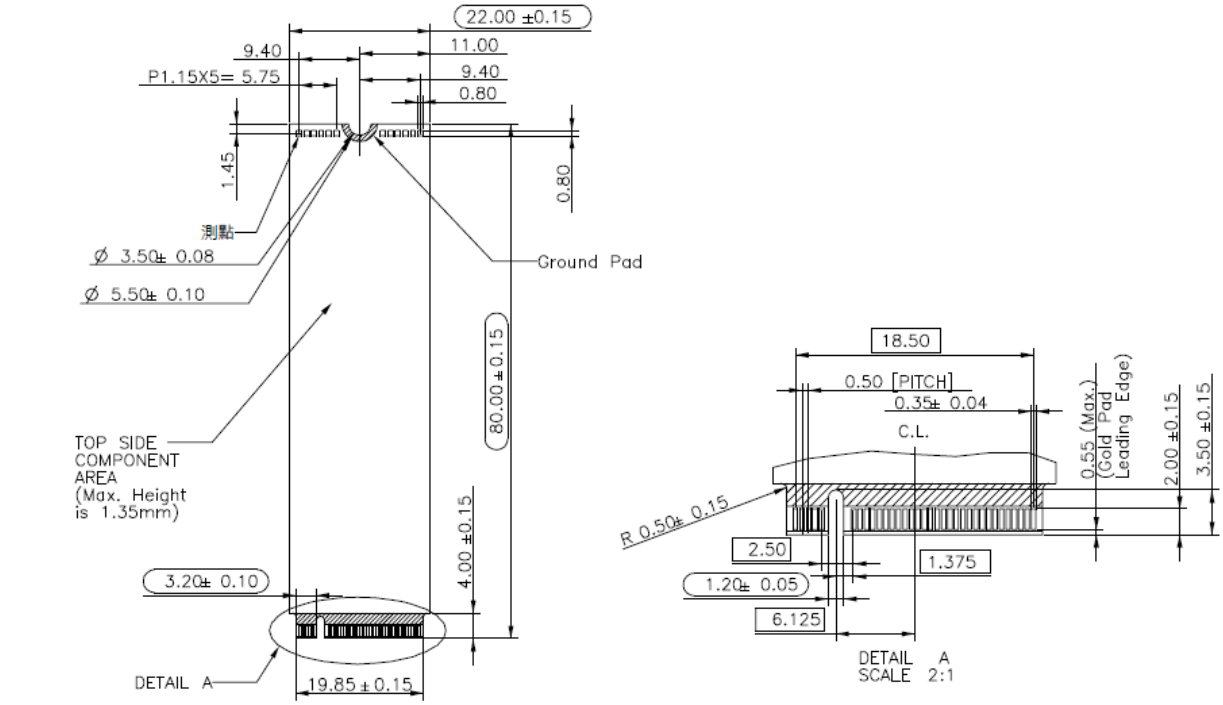
Parameter	Rating
Operating Voltage	3.3V

■ Power Consumption

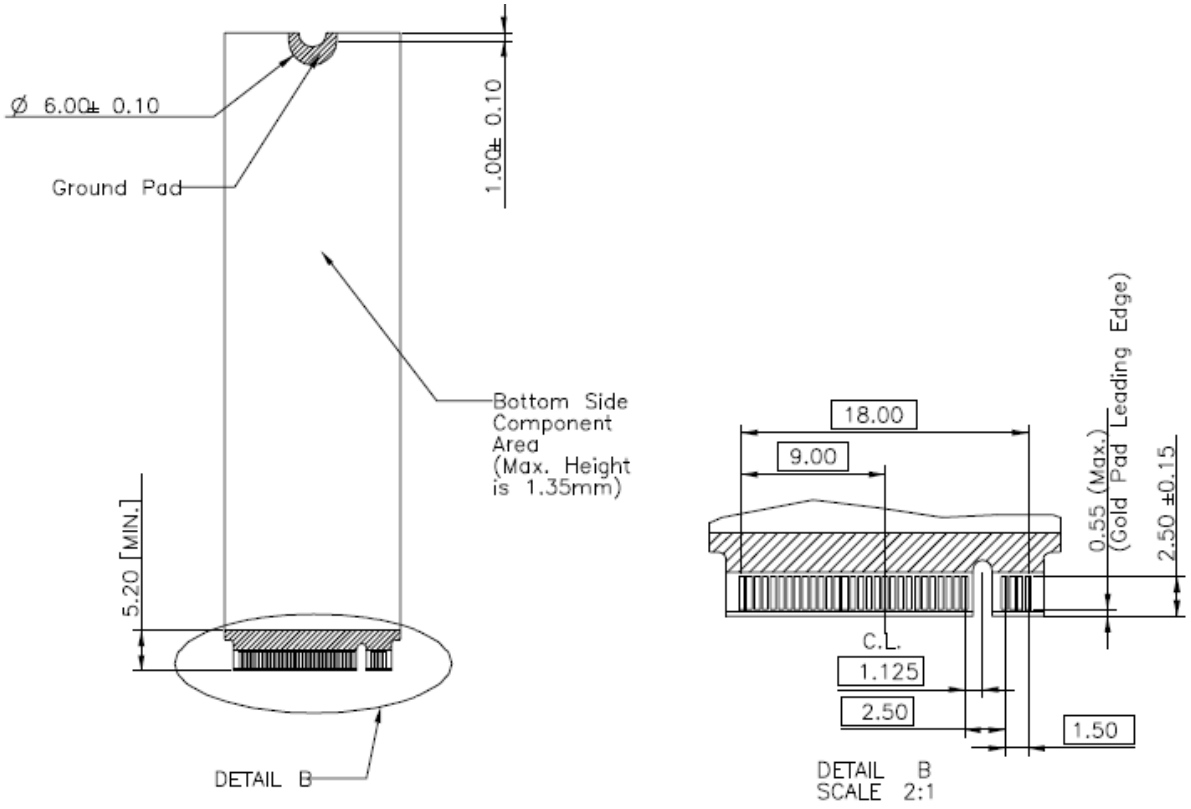
(W)		Read	Write
3D TLC	256 GB	5.0	3.1
	512 GB	5.1	4.5
	1 TB	5.3	4.9

10. Physical Dimension

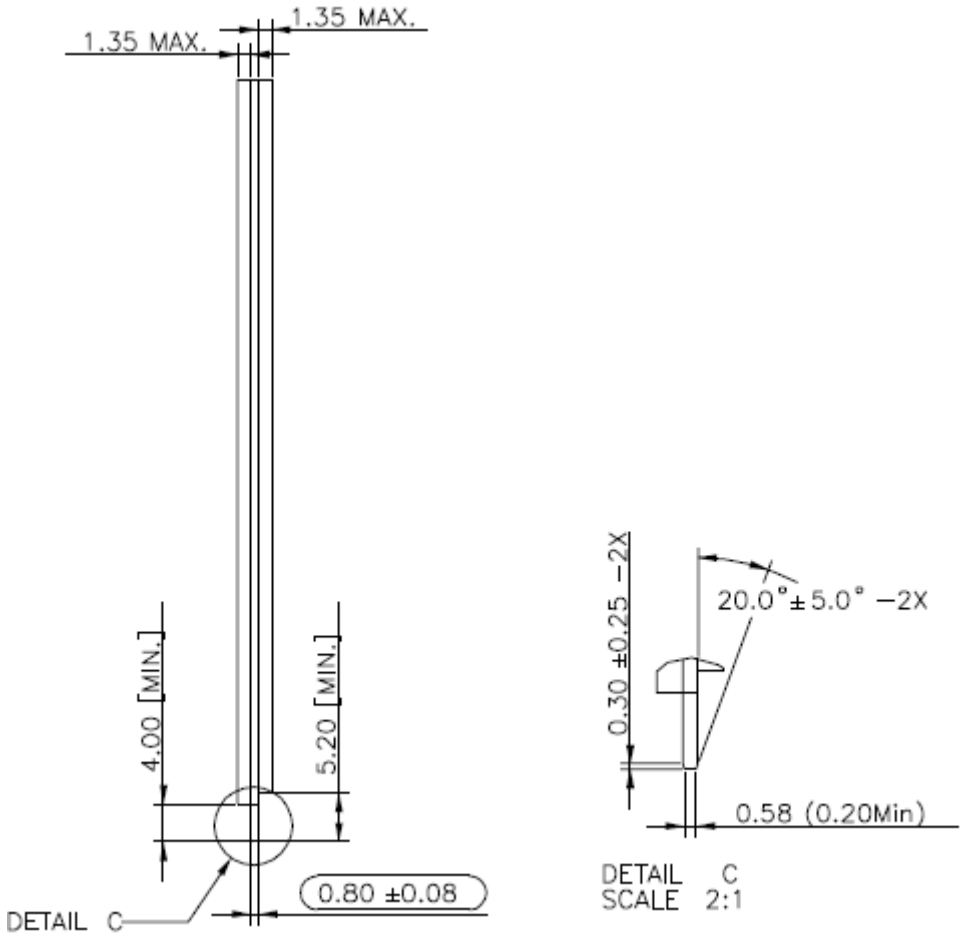
M.2 2280 PCIe SSD (Unit: mm)



Top View



Bottom View


1.35 MAX.
1.35 MAX.
4.00 [MIN.]
5.20 [MIN.]
0.80 ±0.08
DETAIL C
0.30 ±0.25 -2X
20.0° ± 5.0° -2X
0.58 (0.20Min)
DETAIL C
SCALE 2:1

Side View

11. Testing and Certifications

The Advantech SQF 2040 is listed on NIAP, Common Criteria Certified and NSA CSfC listed.

National Information Assurance Partnership (NIAP) - The products listed on the Product Compliant List (PCL) must be considered in the context of the environment of use, including appropriate risk analysis and system accreditation requirements. Customers must ensure that the products selected will provide the necessary security functionality for their architecture.
The products listed on the PCL, are evaluated and granted certificates by NIAP or under CCRA partnering schemes, comply with the requirements of the NIAP program and, where applicable, the requirements of the Federal Information Processing Standard (FIPS) Cryptographic validation program(s). Products on the PCL are evaluated and accredited at licensed/approved evaluation facilities for conformance to the Common Criteria for IT Security Evaluation (ISO Standard 15408). U.S. Customers (designated approving authorities, authorizing officials, integrators, etc.) may treat these mutually-recognized evaluation results as complying with the Committee on National Security Systems Policy (CNSSP) 11, National Policy Governing the Acquisition of Information Assurance (IA) and IA-Enabled Information Technology Products - dated June 2013 (https://www.cnss.gov/CNSS/issuances/Policies.cfm).
NIAP has implemented the CCRA Management Committee Vision Statement for the application of the CC and the CCRA and no longer evaluates against Evaluation Assurance Levels (EAL). This strengthens evaluations by focusing on technology specific security requirements. The products listed below are evaluated against a NIAP-approved Protection Profile, which encompasses the security requirements and test activities suitable across the technology with no EAL assigned - hence the conformance claim is “PP”.

NIAP Product: https://www.niap-ccevs.org/products/11453

Common Criteria Certification

The **Common Criteria for Information Technology Security Evaluation** (referred to as **Common Criteria** or **CC**) is an international standard (ISO/IEC 15408) for computer security certification. It is currently in version 3.1 revision 5.[1]
Common Criteria is a framework in which computer system users can *specify* their security *functional* and *assurance* requirements (SFRs and SARs, respectively) in a Security Target (ST), and may be taken from Protection Profiles (PPs). Vendors can then *implement* or make claims about the security attributes of their products, and testing laboratories can *evaluate* the products to determine if they actually meet the claims. In other words, Common Criteria provides assurance that the process of specification, implementation and evaluation of a computer security product has been conducted in a rigorous and standard and repeatable manner at a level that is commensurate with the target environment for use.[2] Common Criteria maintains a list of certified products, including operating systems, access control systems, databases, and key management systems.[3]

See under other devices and systems: KLC Advantech Drives, Firmware Version: SCPB13.0/ECPB13.0
https://www.commoncriteriaportal.org/products/index.cfm

Common Criteria certificate:
https://www.commoncriteriaportal.org/nfs/ccpfiles/files/epfiles/st_vid11453-ci%20(22).pdf

Certification Report:
https://www.commoncriteriaportal.org/nfs/ccpfiles/files/epfiles/st_vid11453-vr%20(1).pdf

Security Target:
https://www.commoncriteriaportal.org/nfs/ccpfiles/files/epfiles/st_vid11453-st%20(1).pdf

collaborative Protection Profile for Full Drive Encryption - Encryption Engine v2.0 + Errata 201:
https://www.commoncriteriaportal.org/nfs/ccpfiles/files/ppfiles/CPP_FDE_EE_V2.0E.pdf

NSA Commercial Solutions for Classified

This product is eligible to be used as a Hardware Full Disk Encryption Engine component in a CSfC solution.

For more information, please visit:
https://www.nsa.gov/Resources/Commercial-Solutions-for-Classified-Program/

And
https://www.nsa.gov/Resources/Commercial-Solutions-for-Classified-Program/Components-List/#hw-fde

12. Appendix: Part Number Table

Product	KLC PN
M 2 2280 NVMe SSD FIPS 256GB 3D TLC (0~70°C)	SQF-2040-256ECM
M 2 2280 NVMe SSD FIPS 512GB 3D TLC (0~70°C)	SQF-2040-512ECM
M 2 2280 NVMe SSD FIPS 1TB 3D TLC (0~70°C)	SQF-2040-1TECM